AMIS-30522
Micro-Stepping Motor Driver

1.0 Introduction

The AMIS-30522 is a micro-stepping stepper motor driver for bipolar stepper motors. The chip is connected through I/O pins and a SPI interface with an external microcontroller. It has an on-chip voltage regulator, reset-output and watchdog reset, able to supply peripheral devices. AMIS-30522 contains a current-translation table and takes the next micro-step depending on the clock signal on the “NXT” input pin and the status of the “DIR” (=direction) register or input pin. The chip provides a so-called “speed and load angle” output. This allows the creation of stall detection algorithms and control loops based on load-angle to adjust torque and speed. It is using a proprietary PWM algorithm for reliable current control.

The AMIS-30522 is implemented in I2T100 technology, enabling both high-voltage analog circuitry and digital functionality on the same chip. The chip is fully compatible with the automotive voltage requirements.

The AMIS-30522 is ideally suited for general-purpose stepper motor applications in the automotive, industrial, medical, and marine environment. With the on-chip voltage regulator it further reduces the BOM for mechatronic stepper applications.

2.0 Key Features

- Dual H-Bridge for 2-phase stepper motors
- Programmable peak-current up to 1.6A using a 5-bit current DAC
- On-chip current translator
- SPI interface
- Speed and load angle output
- Seven step modes from full step up to 32 micro-steps
- Fully integrated current-sense
- PWM current control with automatic selection of fast and slow decay
- Low EMC PWM with selectable voltage slopes
- Active fly-back diodes
- Full output protection and diagnosis
- Thermal warning and shutdown
- Compatible with 5V and 3.3V microcontrollers
- Integrated 5V regulator to supply external microcontroller
- Integrated reset function to reset external microcontroller
- Integrated watchdog function

3.0 Ordering information

Table 1: Ordering Information

Part Number	Package	Shipping Configuration	Temperature Range	Device/Family Specific #1
AMIS30522C5222G	NQFP-32 (7 x 7mm)	Tube/Tray	-40°C to125°C	1600mA
AMIS30522C5222RG	NQFP-32 (7 x 7mm)	Tape & Reel	-40°C to 125°C	1600mA

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AMIS30522/D

4.0 Block Diagram

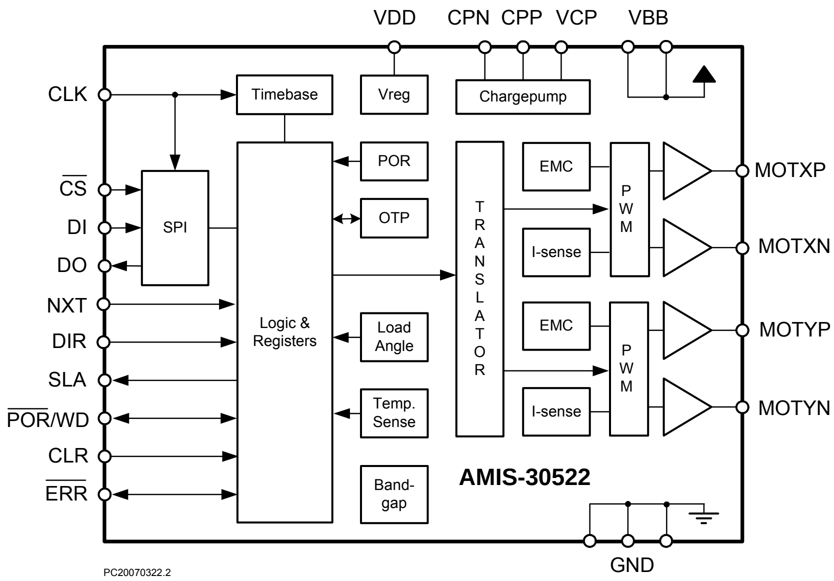

Figure 1: Block Diagram AMIS-30522

5.0 Pin Description

Table 2: Pin List and Description

Name	Pin	Description
DO	31	SPI data output (open drain)
VDD	32	Logic supply output (needs external decoupling capacitor)
GND	1	Ground, heat sink
DI	2	SPI data in
CLK	3	SPI clock input
NXT	4	Next micro-step input
DIR	5	Direction input
ERRB	6	Error output (open drain)
SLA	7	Speed load angle output
CPN	9	Negative connection of charge pump capacitor
CPP	10	Positive connection of charge pump capacitor
VCP	11	Charge pump filter-capacitor
CLR	12	“Clear” = chip reset input
CSB	13	SPI chip select input
VBB	14	High voltage supply Input
MOTYP	15, 16	Negative end of phase Y coil output
GND	17, 18	Ground, heat sink
MOTYN	19, 20	Positive end of phase Y coil output
MOTXN	21, 22	Positive end of phase X coil output
GND	23, 24	Ground, heat sink
MOTXP	25, 26	Negative end of phase X coil output
VBB	27	High voltage supply input
/	8, 30	No function (to be left open in normal operation)
PORB/WD	28	Power-on-reset (POR)and watchdog reset output (open drain)
TSTO	29	Test pin input (to be tied to ground in normal operation)

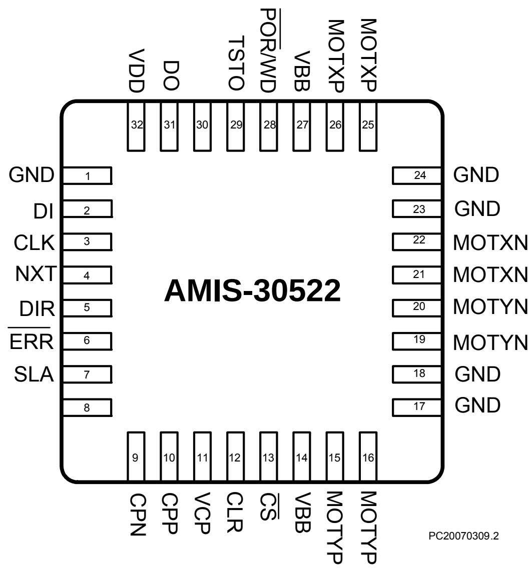

Figure 2: Pin Out AMIS-30522

5.1 Package Thermal Characteristics

The NQFP is designed to provide superior thermal performance, and using an exposed die pad on the bottom surface of the package partly contributes to this. In order to take full advantage of this thermal performance, the PCB must have features to conduct heat away from the package. A thermal grounded pad with thermal via's can achieve this. With a layout as shown in Figure 3, the thermal resistance junction – to – ambient can be brought down to a level of 30°C/W.

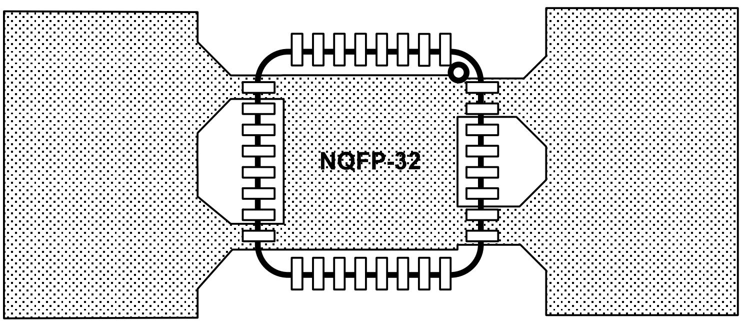

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Figure 3: PCB Ground Plane Layout Condition

6.0 Electrical Specification

6.1 Absolute Maximum Ratings

Stresses above those listed in Table 3 may cause immediate and permanent device failure. It is not implied that more that one of these conditions can be applied simultaneously.

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
V_{BB}	Analog DC supply voltage (1)	-0.3	+40	V
Tstrg	Storage temperature	-55	+160	°C
Tamb	Ambient temperature under bias	-50	+150	°C
V_{ESD}	Electrostatic discharges on component level (2)	-2	+2	kV

Notes:

(1) For limited time <0.5s.

(2) Human body model (100pF via 1.5 kΩ, according to JEDEC EIA-JESD22-A114-B).

6.2 Recommend Operation Conditions

Operating ranges define the limits for functional operation and parametric characteristics of the device. Note that the functionality of the chip outside these operating ranges is not guaranteed. Operating outside the recommended operating ranges for extended periods of time may affect device reliability.

Table 4: Operating Ranges

Symbol	Parameter	Min.	Max.	Units
V_{BB}	Analog DC supply	+6	+30	V
V_{DD}	Logic supply output voltage (1)	4.75	5.25	V
Iddd	Dynamic current of VDD pin (internal and external loads) (2)		18	mA
T_a	Ambient temperature VBAT≤+18	-40	+125	°C
T_a	Ambient temperature VBAT≤+29	-40	+85	°C
T_j	Junction temperature		+160	°C

Notes:

(1) Voltage output.

(2) Dynamic current is with oscillator running, all analog cells active. All outputs unloaded, no floating inputs.

6.3 DC Parameters

The DC parameters are given for V_{BB} and temperature in their operating ranges unless otherwise specified. Convention: currents flowing in the circuit are defined as positive.

Table 5: DC parameters

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
Supply & Voltage Regulator							
V_{BB}	VBB	Nominal operating supply range		6		30	V
I_{BB}		Total internal current consumption	Unloaded outputs			8	mA
V_{DD}	VDD	Regulated Output Voltage		4.75	5	5.25	V
I_{INT}		Internal load current	Unloaded outputs				
I_{LOAD}		Max. Output Current (external and internal loads)	6V < V_{BB} < 8V	20			
			8V < V_{BB} < 30V	50			
I_{DDLIM}		Current limitation	Pin shorted to ground			150	mA
I_{LOAD_PD}		Output current in Power Down		1			
Power-on-Reset (POR)							
V_{DDH}	VDD	Internal POR comparator threshold	VDD rising	4.0	4.25	4.4	V
V_{DDL}		Internal POR comparator threshold	VDD falling		3.68		V
Motor Driver							
$I_{MDmax,Peak}$	MOTXP MOTXN MOTYP MOTYN	Max current through motor coil in normal operation			1600		mA
$I_{MDmax,RMS}$		Max RMS current through coil in normal operation			800		mA
I_{MDabs}		Absolute error on coil current		-10		10	%
I_{MDrel}		Error on current ratio I_{coilx} / I_{coily}		-7		7	%
I_{SET_TC1}		Temperature coefficient of coil current set-level, CUR[4:0] = 0 ..27	-40 °C ≤ T_j ≤ 160 °C		-240		ppm/K
I_{SET_TC2}		Temperature coefficient of coil current set-level, CUR[4:0] = 28 ..31	-40 °C ≤ T_j ≤ 160 °C		-490		ppm/K
R_{HS}		On-resistance high-side driver, CUR[4:0] = 0...31	V_{bb} = 12V, T_j = 27 °C		0.45	0.56	Ω
			V_{bb} = 12V, T_j = 160 °C		0.94	1.25	Ω
R_{LS3}		On-resistance low-side driver, CUR[4:0] = 23...31	V_{bb} = 12V, T_j = 27 °C		0.45	0.56	Ω
			V_{bb} = 12V, T_j = 160 °C		0.94	1.25	Ω
R_{LS2}		On-resistance low-side driver, CUR[4:0] = 16...22	V_{bb} = 12V, T_j = 27 °C		0.90	1.2	Ω
			V_{bb} = 12V, T_j = 160 °C		1.9	2.5	Ω
R_{LS1}		On-resistance low-side driver, CUR[4:0] = 9...15	V_{bb} = 12V, T_j = 27 °C		1.8	2.3	Ω
			V_{bb} = 12V, T_j = 160 °C		3.8	5.0	Ω
R_{LS0}		On-resistance low-side driver, CUR[4:0] = 0...8	V_{bb} = 12V, T_j = 27 °C		3.6	4.5	Ω
			V_{bb} = 12V, T_j = 160 °C		7.5	10	Ω
I_{Mpd}		Pull down current	HiZ mode		0.5		mA
Digital Inputs							
I_{leak}	DI, CLK NXT, DIR CLR, CSB	Input Leakage (3)	Tj = 160 °C			1	µA
V_{IL}		Logic Low Threshold		0		0.65	V
V_{IH}		Logic High Threshold		2.20		V_{DD}	V
R_{pd_CLR}	CLR	Internal Pull Down Resistor		120		300	kΩ
R_{pd_TST}	TST0	Internal Pull Down Resistor		3		9	kΩ
Digital Outputs							
V_{OL}	DO, ERRB, PORB/WD	Logic Low level open drain	IOL = 5 mA			0.5	V
Thermal Warning & Shutdown							
T_{tw}		Thermal Warning		138	145	152	°C
T_{tsd}(1) (2)		Thermal shutdown			T_{tw} + 20		°C
Charge Pump							
V_{cp}	VCP	Output voltage	6V< V_{BB} < 15V		2 * V_{BB} – 2.5		V
			15V < V_{BB} < 30V	V_{BB}+12.5	V_{BB}+14	V_{BB}+15.5	V
C_{buffer}		External buffer capacitor		180	220	470	nF
C_{pump}	CPP CPN	External pump capacitor		180	220	470	nF

Notes:

(1) No more than 100 cumulated hours in life time above Tt_w.

(2) Thermal shutdown and low temperature warning are derived from thermal warning.

(3) Not valid for pins with internal pull-down resistor.

6.4 AC Parameters

The AC parameters are given for V_{BB} and temperature in their operating ranges.

Table 6: AC Parameters

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min.	Typ.	Max.	Unit
Internal Oscillator							
f_{osc}		Frequency of internal oscillator		3.6	4	4.4	MHz
Motor Driver							
f_{PWM}	MOTxx	PWM frequency	Frequency depends only on internal oscillator	20.8	22.8	24.8	kHz
		Double PWM frequency		41.6	45.6	49.6	kHz
f_j		PWM jitter frequency			tbd		Hz
f_d		PWM jitter Depth			tbd		% f_{PWM}
Tb_{rise}	MOTxx	Turn-on voltage slope, 10% to 90%	EMC[1:0] = 00		150		V/µs
			EMC[1:0] = 01		100		V/µs
			EMC[1:0] = 10		50		V/µs
			EMC[1:0] = 11		25		V/µs
Tb_{fall}	MOTxx	Turn-off voltage slope, 90% to 10%	EMC[1:0] = 00		150		V/µs
			EMC[1:0] = 01		100		V/µs
			EMC[1:0] = 10		50		V/µs
			EMC[1:0] = 11		25		V/µs
Digital Outputs							
T_{H2L}	DO ERRB	Output fall-time from V_{inH} to V_{inL}	Capacitive load 400pF and pull-up resistor of 1.5 kΩ			50	ns
Charge Pump							
f_{CP}	CPN CPP	Charge pump frequency			250		kHz
T_{CPU}	MOTxx	Start-up time of charge pump	Spec external components				
CLR Function							
T_{CLR}	CLR	Hard reset duration time		20		90	µs
Power-Up							
t_{PU}	PORB/ WD	Power-up time	V_{BB}=12V, I_{LOAD}=50mA, C_{LOAD}=220nF			110	µs
t_{PD}		Power-down time	External conditions tbd				ms
t_{POR}		Reset duration			100		ms
t_{RF}		Reset filter time			1		µs
Watchdog							
t_{WDTO}	PORB/ WD	Watchdog time out interval		32		512	ms
t_{WDPR}		Prohibited watchdog acknowledge delay			2		ms
t_{WDRD}		Watchdog reset delay			tbd		µs

6.5 SPI Timing

Table 7: SPI Timing Parameters

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CLK}	SPI clock period	1			µs
t_{CLK_HIGH}	SPI clock high time	100			ns
t_{CLK_LOW}	SPI clock low time	100			ns
t_{SET_DI}	DI set up time, valid data before rising edge of CLK	50			ns
t_{HOLD_DI}	DI hold time, hold data after rising edge of CLK	50			ns
t_{CSB_HIGH}	CSB high time	2.5			µs
t_{SET_CSB}	CSB set up time, CSB low before rising edge of CLK	100			ns
t_{SET_CLK}	CLK set up time, CLK low before rising edge of CSB	100			ns

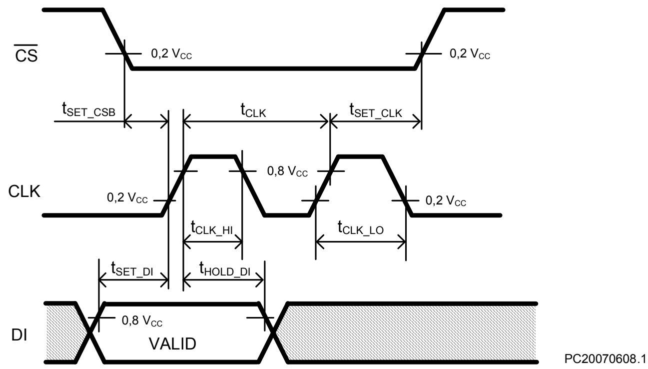


Figure 4: SPI Timing

7.0 Typical Application Schematic

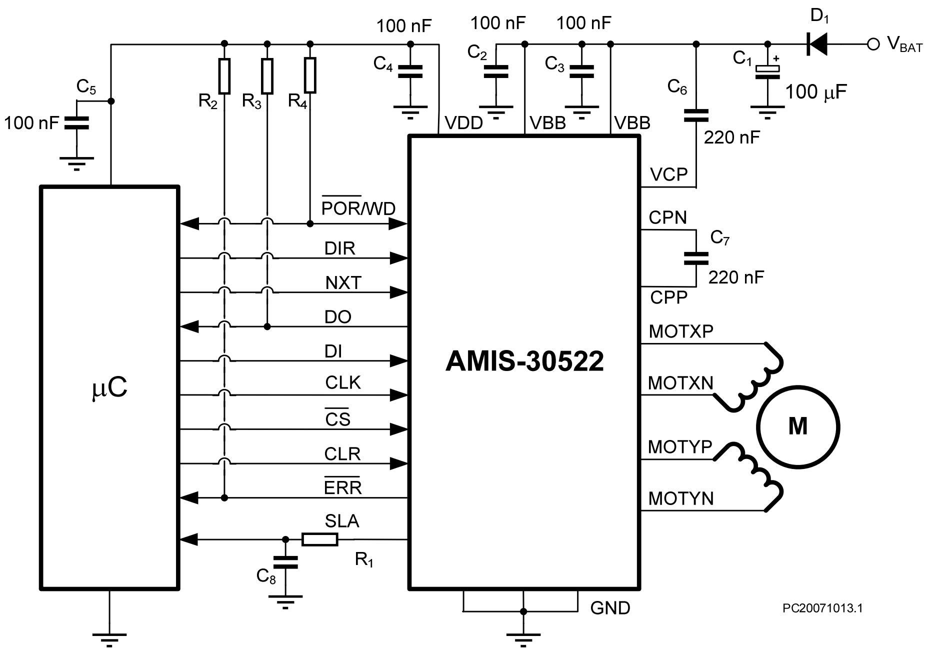


Figure 5: Typical Application Schematic AMIS-30522

Table 8: External Components List and Description

Component	Function	Typ. Value	Tolerance	Unit
C_1	V_{BB} buffer capacitor (1)	100	-20 +80%	µF
C_2, C_3	V_{BB} decoupling block capacitor	100	-20 +80%	nF
C_4	V_{DD} buffer capacitor	220	+/- 20 %	nF
C_5	V_{DD} buffer capacitor	100	+/- 20%	nF
C_6	Charge-pump buffer capacitor	220	+/- 20%	nF
C_7	Charge-pump pumping capacitor	220	+/- 20%	nF
C_8	Low pass filter SLA	1	+/- 20%	nF
R_1	Low pass filter SLA	5.6	+/- 1%	kΩ
R_2, R_3, R_4	Pull up resistor open drain output	4,7	+/- 1%	kΩ
D_1	Optional reverse protection diode	e.g. 1N4003		

Notes:

1. Low ESR < 1Ohm.

8.0 Functional Description

8.1 H-Bridge Drivers

A full H-bridge is integrated for each of the two stator windings. Each H-bridge consists of two low-side and two high-side N-type MOSFET switches. Writing logic '0' in bit <MOTEN> disables all drivers (high-impedance). Writing logic '1' in this bit enables both bridges and current can flow in the motor stator windings.

In order to avoid large currents through the H-bridge switches, it is guaranteed that the top- and bottom-switches of the same half-bridge are never conductive simultaneously (interlock delay).

A two-stage protection against shorts on motor lines is implemented. In a first stage, the current in the driver is limited. Secondly, when excessive voltage is sensed across the transistor, the transistor is switched off.

In order to reduce the radiated/conducted emission, voltage slope control is implemented in the output switches. The output slope is defined by the gate-drain capacitance of output transistor and the (limited) current that drives the gate. There are two trimming bits for slope control (see Table 27).

The power transistors are equipped with so-called "active diodes": when a current is forced trough the transistor switch in the reverse direction, i.e. from source to drain, then the transistor is switched on. This ensures that most of the current flows through the channel of the transistor instead of through the inherent parasitic drain-bulk diode of the transistor.

Depending on the desired current range and the micro-step position at hand, the Rdson of the low-side transistors will be adapted such that excellent current-sense accuracy is maintained. The Rdson of the high-side transistors remain unchanged, see **Error! Reference source not found.** for more details.

8.2 PWM Current Control

A PWM comparator compares continuously the actual winding current with the requested current and feeds back the information to a digital regulation loop. This loop then generates a PWM signal, which turns on/off the H-bridge switches. The switching points of the PWM duty-cycle are synchronized to the on-chip PWM clock. The frequency of the PWM controller can be doubled and an artificial jitter can be added (see Table 16). The PWM frequency will not vary with changes in the supply voltage. Also variations in motor-speed or load-conditions of the motor have no effect. There are no external components required to adjust the PWM frequency.

8.2.1. Automatic Forward and Slow-Fast Decay

The PWM generation is in steady-state using a combination of forward and slow-decay. The absence of fast-decay in this mode, guarantees the lowest possible current-ripple "by design". For transients to lower current levels, fast-decay is automatically activated to allow high-speed response. The selection of fast or slow decay is completely transparent for the user and no additional parameters are required for operation.

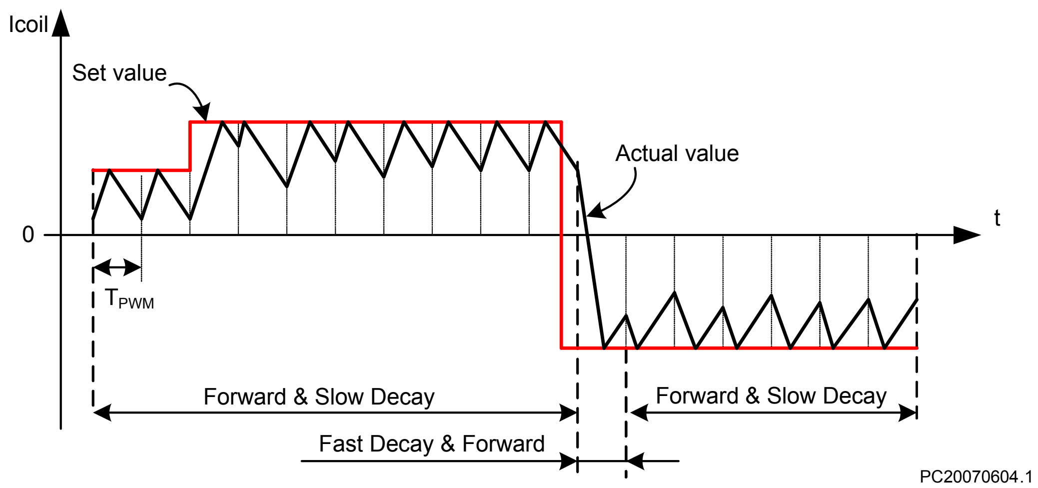


Figure 6: Forward and Slow/Fast Decay PWM

8.2.2. Automatic Duty Cycle Adaptation

In case the supply voltage is lower than 2*Bemf, then the duty cycle of the PWM is adapted automatically to >50% to maintain the requested average current in the coils. This process is completely automatic and requires no additional parameters for operation. The over-all current-ripple is divided by two if PWM frequency is doubled (see Table 16).

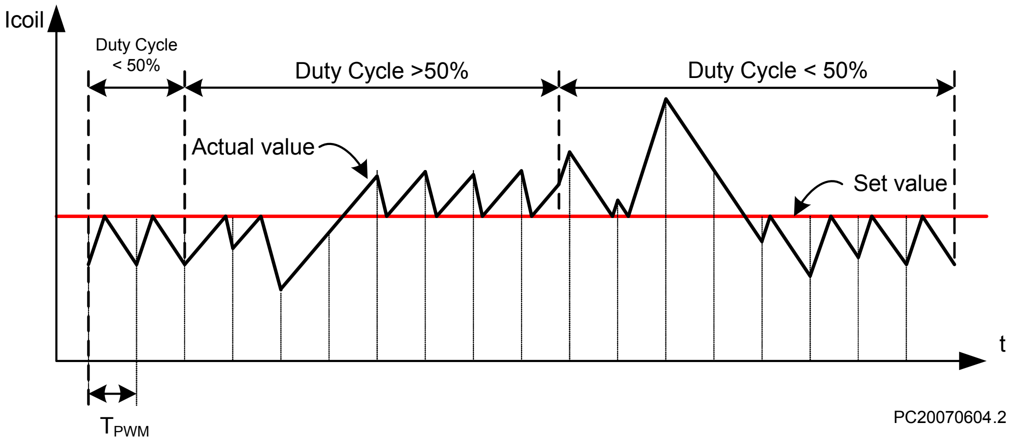


Figure 7: Automatic Duty Cycle Adaptation

8.3 Step Translator

8.3.1. Step Mode

The step translator provides the control of the motor by means of SPI register Stepmode: SM[2:0], SPI register DIRCNTRL, and input pins DIR and NXT. It is translating consecutive steps in corresponding currents in both motor coils for a given step mode.

One out of seven possible stepping modes can be selected through SPI-bits SM[2:0] (see Table 28) After power-on or hard reset, the coil-current translator is set to the default 1/32 micro-stepping at position **'0'**. Upon changing the step mode, the translator jumps to position **0*** of the corresponding stepping mode. When remaining in the same step mode, subsequent translator positions are all in the same column and increased or decreased with 1. **Error! Reference source not found.** lists the output current vs. the translator position.

As shown in Figure 8 the output current-pairs can be projected approximately on a circle in the (I_x,I_y) plane. There is, however, one exception: uncompensated half step. In this step mode the currents are not regulated to a fraction of Imax but are in all intermediate steps regulated at 100 percent. In the (I_x,I_y) plane the current-pairs are projected on a square. **Error! Reference source not found.** lists the output current vs. the translator position for this case.

Table 9: Square Translator Table for Full Step and Uncompensated Half Step

MSP[6:0]	Stepmode (SM[2:0])		% of Imax	
	101	110	Coil x	Coil y
	Uncompensated Half-Step	Full Step		
000 0000	**0***	-	0	100
001 0000	1	1	100	100
010 0000	2	-	100	0
011 0000	3	2	100	-100
100 0000	4	-	0	-100
101 0000	5	3	-100	-100
110 0000	6	-	-100	0
111 0000	7	**0***	-100	100

Table 10: Circular Translator Table

MSP[6:0]	Stepmode (SM[2:0])					% of Imax		MSP[6:0]	Stepmode (SM[2:0])					% of Imax	
	000	001	010	011	100	Coil x	Coil y		000	001	010	011	100	Coil x	Coil y
	1/32	1/16	1/8	1/4	1/2				1/32	1/16	1/8	1/4	1/2		
000 0000	**‘0’**	**0***	**0***	**0***	**0***	**0**	**100**	100 0000	64	32	16	8	4	**0**	**-100**
000 0001	1	-	-	-	-	**3.5**	**98.8**	100 0001	65	-	-	-	-	**-3.5**	**-98.8**
000 0010	2	1	-	-	-	**8.1**	**97.7**	100 0010	66	33	-	-	-	**-8.1**	**-97.7**
000 0011	3	-	-	-	-	**12.7**	**96.5**	100 0011	67	-	-	-	-	**-12.7**	**-96.5**
000 0100	4	2	1	-	-	**17.4**	**95.3**	100 0100	68	34	17	-	-	**-17.4**	**-95.3**
000 0101	5	-	-	-	-	**22.1**	**94.1**	100 0101	69	-	-	-	-	**-22.1**	**-94.1**
000 0110	6	3	-	-	-	**26.7**	**93**	100 0110	70	35	-	-	-	**-26.7**	**-93**
000 0111	7	-	-	-	-	**31.4**	**91.8**	100 0111	71	-	-	-	-	**-31.4**	**-91.8**
000 1000	8	4	2	1	-	**34.9**	**89.5**	100 1000	72	36	18	9	-	**-34.9**	**-89.5**
000 1001	9	-	-	-	-	**38.3**	**87.2**	100 1001	73	-	-	-	-	**-38.3**	**-87.2**
000 1010	10	5	-	-	-	**43**	**84.9**	100 1010	74	37	-	-	-	**-43**	**-84.9**
000 1011	11	-	-	-	-	**46.5**	**82.6**	100 1011	75	-	-	-	-	**-46.5**	**-82.6**
000 1100	12	6	3	-	-	**50**	**79**	100 1100	76	38	19	-	-	**-50**	**-79**
000 1101	13	-	-	-	-	**54.6**	**75.5**	100 1101	77	-	-	-	-	**-54.6**	**-75.5**
000 1110	14	7	-	-	-	**58.1**	**72.1**	100 1110	78	39	-	-	-	**-58.1**	**-72.1**
000 1111	15	-	-	-	-	**61.6**	**68.6**	100 1111	79	-	-	-	-	**-61.6**	**-68.6**
001 0000	16	8	4	2	1	**65.1**	**65.1**	101 0000	80	40	20	10	5	**-65.1**	**-65.1**
001 0001	17	-	-	-	-	**68.6**	**61.6**	101 0001	81	-	-	-	-	**-68.6**	**-61.6**
001 0010	18	9	-	-	-	**72.1**	**58.1**	101 0010	82	41	-	-	-	**-72.1**	**-58.1**
001 0011	19	-	-	-	-	**75.5**	**54.6**	101 0011	83	-	-	-	-	**-75.5**	**-54.6**
001 0100	20	10	5	-	-	**79**	**50**	101 0100	84	42	21	-	-	**-79**	**-50**
001 0101	21	-	-	-	-	**82.6**	**46.5**	101 0101	85	-	-	-	-	**-82.6**	**-46.5**
001 0110	22	11	-	-	-	**84.9**	**43**	101 0110	86	43	-	-	-	**-84.9**	**-43**
001 0111	23	-	-	-	-	**87.2**	**38.3**	101 0111	87	-	-	-	-	**-87.2**	**-38.3**
001 1000	24	12	6	3	-	**89.5**	**34.9**	101 1000	88	44	22	11	-	**-89.5**	**-34.9**
001 1001	25	-	-	-	-	**91.8**	**31.4**	101 1001	89	-	-	-	-	**-91.8**	**-31.4**
001 1010	26	13	-	-	-	**93**	**26.7**	101 1010	90	45	-	-	-	**-93**	**-26.7**
001 1011	27	-	-	-	-	**94.1**	**22.1**	101 1011	91	-	-	-	-	**-94.1**	**-22.1**
001 1100	28	14	7	-	-	**95.3**	**17.4**	101 1100	92	46	23	-	-	**-95.3**	**-17.4**
001 1101	29	-	-	-	-	**96.5**	**12.7**	101 1101	93	-	-	-	-	**-96.5**	**-12.7**
001 1110	30	15	-	-	-	**97.7**	**8.1**	101 1110	94	47	-	-	-	**-97.7**	**-8.1**
001 1111	31	-	-	-	-	**98.8**	**3.5**	101 1111	95	-	-	-	-	**-98.8**	**-3.5**
010 0000	32	16	8	4	2	**100**	**0**	110 0000	96	48	24	12	6	**-100**	**0**
010 0001	33	-	-	-	-	**98.8**	**-3.5**	110 0001	97	-	-	-	-	**-98.8**	**3.5**
010 0010	34	17	-	-	-	**97.7**	**-8.1**	110 0010	98	49	-	-	-	**-97.7**	**8.1**
010 0011	35	-	-	-	-	**96.5**	**-12.7**	110 0011	99	-	-	-	-	**-96.5**	**12.7**
010 0100	36	18	9	-	-	**95.3**	**-17.4**	110 0100	100	50	25	-	-	**-95.3**	**17.4**
010 0101	37	-	-	-	-	**94.1**	**-22.1**	110 0101	101	-	-	-	-	**-94.1**	**22.1**
010 0110	38	19	-	-	-	**93**	**-26.7**	110 0110	102	51	-	-	-	**-93**	**26.7**
010 0111	39	-	-	-	-	**91.8**	**-31.4**	110 0111	103	-	-	-	-	**-91.8**	**31.4**
010 1000	40	20	10	5	-	**89.5**	**-34.9**	110 1000	104	52	26	13	-	**-89.5**	**34.9**
010 1001	41	-	-	-	-	**87.2**	**-38.3**	110 1001	105	-	-	-	-	**-87.2**	**38.3**
010 1010	42	21	-	-	-	**84.9**	**-43**	110 1010	106	53	-	-	-	**-84.9**	**43**
010 1011	43	-	-	-	-	**82.6**	**-46.5**	110 1011	107	-	-	-	-	**-82.6**	**46.5**
010 1100	44	22	11	-	-	**79**	**-50**	110 1100	108	54	27	-	-	**-79**	**50**
010 1101	45	-	-	-	-	**75.5**	**-54.6**	110 1101	109	-	-	-	-	**-75.5**	**54.6**
010 1110	46	23	-	-	-	**72.1**	**-58.1**	110 1110	110	55	-	-	-	**-72.1**	**58.1**
010 1111	47	-	-	-	-	**68.6**	**-61.6**	110 1111	111	-	-	-	-	**-68.6**	**61.6**
011 0000	48	24	12	6	3	**65.1**	**-65.1**	111 0000	112	56	28	14	7	**-65.1**	**65.1**
011 0001	49	-	-	-	-	**61.6**	**-68.6**	111 0001	113	-	-	-	-	**-61.6**	**68.6**
011 0010	50	25	-	-	-	**58.1**	**-72.1**	111 0010	114	57	-	-	-	**-58.1**	**72.1**
011 0011	51	-	-	-	-	**54.6**	**-75.5**	111 0011	115	-	-	-	-	**-54.6**	**75.5**
011 0100	52	26	13	-	-	**50**	**-79**	111 0100	116	58	29	-	-	**-50**	**79**
011 0101	53	-	-	-	-	**46.5**	**-82.6**	111 0101	117	-	-	-	-	**-46.5**	**82.6**
011 0110	54	27	-	-	-	**43**	**-84.9**	111 0110	118	59	-	-	-	**-43**	**84.9**
011 0111	55	-	-	-	-	**38.3**	**-87.2**	111 0111	119	-	-	-	-	**-38.3**	**87.2**
011 1000	56	28	14	7	-	**34.9**	**-89.5**	111 1000	120	60	30	15	-	**-34.9**	**89.5**
011 1001	57	-	-	-	-	**31.4**	**-91.8**	111 1001	121	-	-	-	-	**-31.4**	**91.8**
011 1010	58	29	-	-	-	**26.7**	**-93**	111 1010	122	61	-	-	-	**-26.7**	**93**
011 1011	59	-	-	-	-	**22.1**	**-94.1**	111 1011	123	-	-	-	-	**-22.1**	**94.1**
011 1100	60	30	15	-	-	**17.4**	**-95.3**	111 1100	124	62	31	-	-	**-17.4**	**95.3**
011 1101	61	-	-	-	-	**12.7**	**-96.5**	111 1101	125	-	-	-	-	**-12.7**	**96.5**
011 1110	62	31	-	-	-	**8.1**	**-97.7**	111 1110	126	63	-	-	-	**-8.1**	**97.7**
011 1111	63	-	-	-	-	**3.5**	**-98.8**	111 1111	127	-	-	-	-	**-3.5**	**98.8**

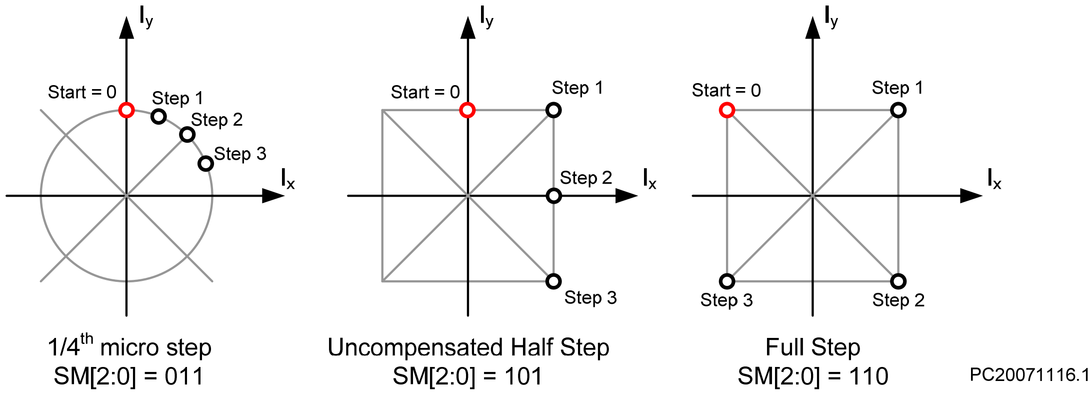


Figure 8: Translator Table: Circular and Square

8.3.2. Direction

The direction of rotation is selected by means of following combination of the DIR input pin and the SPI-controlled direction bit `<DIRCTRL>`. (Table 16)

8.3.3. NXT input

Changes on the NXT input will move the motor current one step up/down in the translator table. Depending on the NXT-polarity bit `<NXTP>` (Table 16), the next step is initiated either on the rising edge or the falling edge of the NXT input.

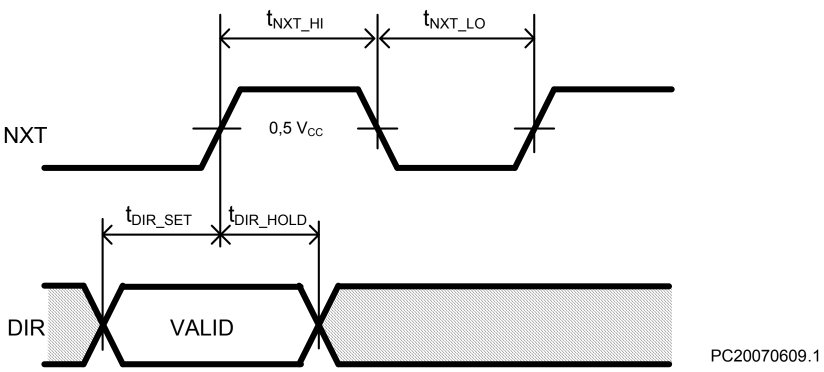


Figure 9: NXT-input Timing Diagram

Table 11: Timing Table NXT Pin

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{NXT_HI}	NXT minimum, high pulse width	2			μs
t_{NXT_LO}	NXT minimum, low pulse width	2			μs
t_{DIR_SET}	NXT hold time, following change of DIR	0.5			μs
t_{DIR_HOLD}	NXT hold time, before change of DIR	0.5			μs

8.3.4. Translator Position

The translator position can be read in Table 32. This is a 7-bit number equivalent to the 1/32th micro-step from **Error! Reference source not found.**. The translator position is updated immediately following a NXT trigger.

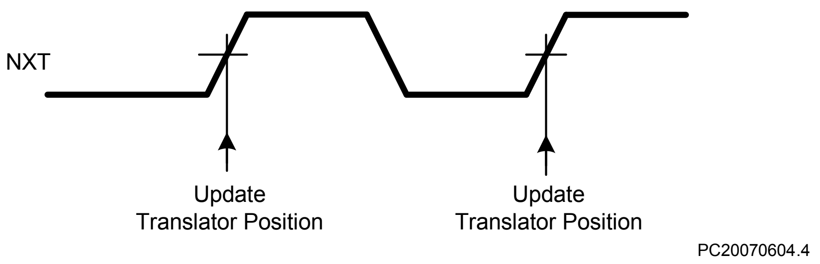


Figure 10: Translator Position Timing Diagram

8.3.5. Synchronization of Step Mode and NXT Input

When step mode is re-programmed to another resolution (Table 15), then this is put in effect immediately upon the first arriving "NXT" input. If the micro-stepping resolution is increased (Figure 11), then the coil currents will be regulated to the nearest micro-step, according to the fixed grid of the increased resolution. If however the micro-stepping resolution is decreased, then it is possible to introduce an offset (or phase shift) in the micro-step translator table.

If the step resolution is decreased at a translator table position that is shared both by the old and new resolution setting, then the offset is zero and micro-stepping is proceeds according to the translator table.

If the translator position is **not** shared both by the old and new resolution setting, then the micro-stepping proceeds with an offset relative to the translator table (See Figure 10 right hand side).

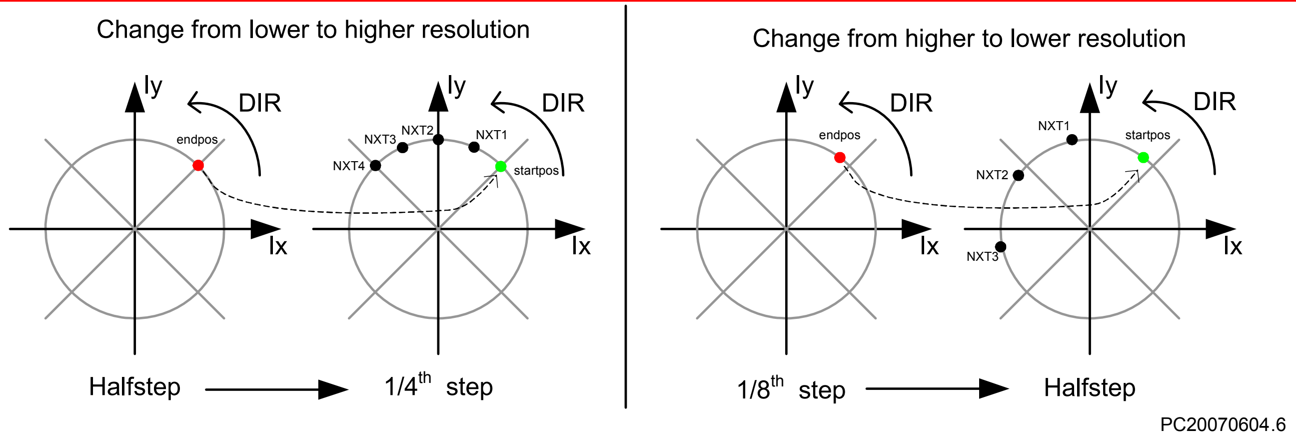


Figure 11: NXT-Step Mode Synchronization

Left: Change from lower to higher resolution. The left-hand side depicts the ending half-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the micro-step position.

Right: Change from higher to lower resolution. The left-hand side depicts the ending micro-step position during which a new step mode resolution was programmed. The right-hand side diagram shows the effect of subsequent NXT commands on the half-step position.

Note:
It is advised to reduce the micro-stepping resolution only at micro-step positions that overlap with desired micro-step positions of the new resolution.

8.4 Programmable Peak-Current

The amplitude of the current waveform in the motor coils (coil peak current = Imax) is adjusted by means of an SPI parameter "CUR[4:0]" (Table 15). Whenever this parameter is changed, the coil-currents will be updated immediately at the next PWM period. More information can be found in Table 26.

8.5 Speed and Load Angle Output

The SLA-pin provides an output voltage that indicates the level of the Back-e.m.f. voltage of the motor. This Back-e.m.f. voltage is sampled during every so-called "coil current zero crossings". Per coil, two zero-current positions exist per electrical period, yielding in total four zero-current observation points per electrical period.

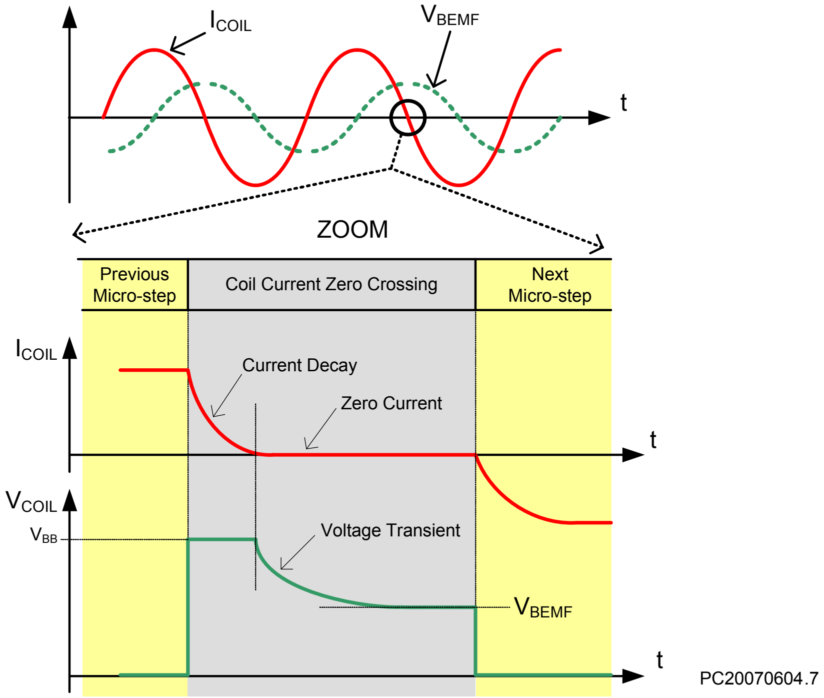


Figure 12: Principle of Bemf Measurement

Because of the relatively high recirculation currents in the coil during current decay, the coil voltage V_{COIL} shows a transient behavior. As this transient is not always desired in application software, two operating modes can be selected by means of the bit <SLAT> (see "SLA-transparency" in Table 17). The SLA pin shows in "transparent mode" full visibility of the voltage transient behavior. This allows a sanity-check of the speed-setting versus motor operation and characteristics and supply voltage levels. If the bit "SLAT" is cleared, then only the voltage samples at the end of each coil current zero crossing are visible on the SLA-pin. Because the transient behavior of the coil voltage is not visible anymore, this mode generates smoother Back e.m.f. input for post-processing, e.g. by software.

In order to bring the sampled Back e.m.f. to a descent output level (0 to 5V), the sampled coil voltage V_{COIL} is divided by 2 or by 4. This divider is set through an SPI bit <SLAG>. (Table 17)

Table 12: Parameter Table SLA Pin

Symbol	Pin(s)	Parameter	Remark/Test Conditions	Min	Typ	Max	Unit
V_{out}	SLA	Output voltage range		0.5		4.5	V
V_{off}		Output offset the SLA pin	0.2V < Vsla < Vdd – 0.2V	-25		25	mV
R_{out}		Output resistance SLA pin				1	kΩ
C_{load}		Load capacitance SLA pin				50	pF
G_{sla}		Gain of SLA pin = V_{BEMF} / V_{COIL}	SLAG=0 SLAG=1		0.5 0.25		

The following drawing illustrates the operation of the SLA-pin and the transparency-bit. "PWMsh" and "Icoil=0" are internal signals that define together with SLAT the sampling and hold moments of the coil voltage.

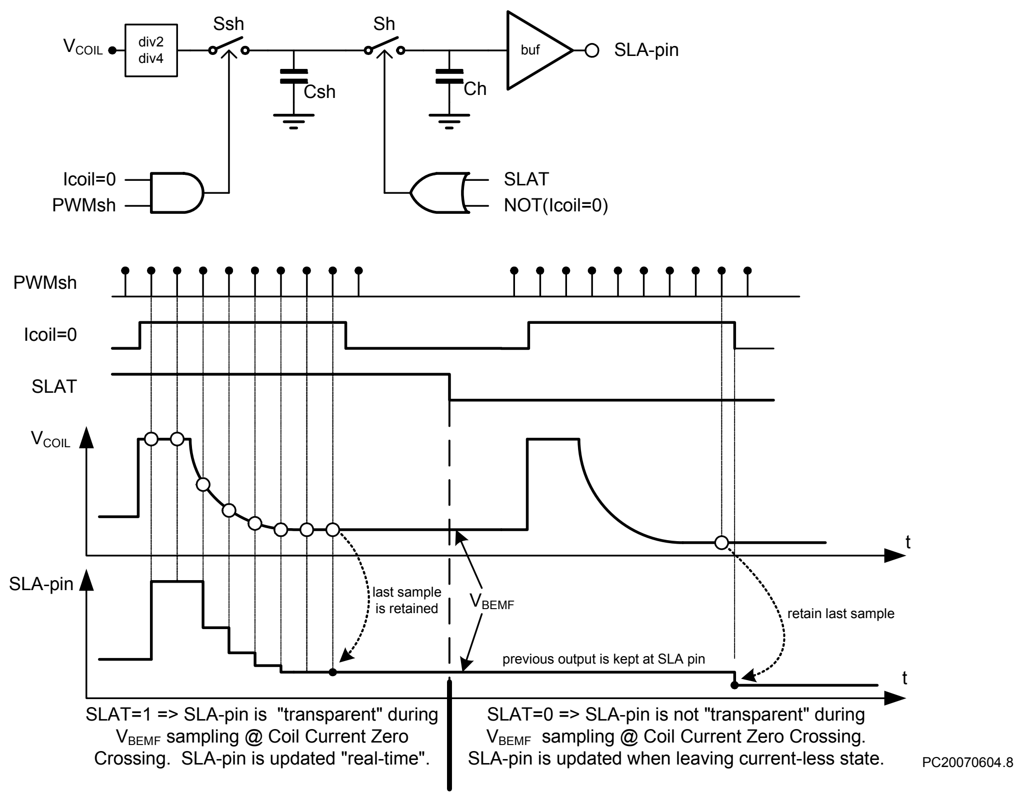


Figure 13: Timing Diagram of SLA-pin

8.6 Warning, Error Detection and Diagnostics Feedback

8.6.1. Thermal Warning and Shutdown

When junction temperature rises above T_{TW}, the thermal warning bit <TW> is set (Table 29). If junction temperature increases above thermal shutdown level, then the circuit goes in "Thermal Shutdown" mode (<TSD>) and all driver transistors are disabled (high impedance) (Table 31). The conditions to reset flag <TSD> is to be at a temperature lower than T_{TW} and to clear the <TSD> flag by reading it using any SPI read command.

8.6.2. Over-Current Detection

The over-current detection circuit monitors the load current in each activated output stage. If the load current exceeds the over-current detection threshold, then the over-current flag is set and the drivers are switched off to reduce the power dissipation and to protect the integrated circuit. Each driver transistor has an individual detection bit in

Table 30 and (Table 31(<OVCXij> and <OVCYij>). Error condition is latched and the microcontroller needs to clean the status bits to reactivate the drivers.

8.6.3. Open Coil Detection

Open coil detection is based on the observation of 100 percent duty cycle of the PWM regulator. If in a coil 100 percent duty cycle is detected for longer than 200ms then the related driver transistors are disabled (high-impedance) and an appropriate bit in the SPI status register is set (<OPENX> or <OPENY>). (Table 29)

8.6.4. Charge Pump Failure

The charge pump is an important circuit that guarantees low Rdson for all drivers, especially for low supply voltages. If supply voltage is too low or external components are not properly connected to guarantee Rdson of the drivers, then the bit <CPFAIL> is set in Table 29. Also after POR the charge pump voltage will need some time to exceed the required threshold. During that time <CPFAIL> will be set to "1".

8.6.5. Error Output

This is a digital output to flag a problem to the external microcontroller. The signal on this output is active low and the logic combination of:

NOT(ERRB) = <TW> OR <TSD> OR <OVCXij> OR < OVCYij> OR <OPENi> OR <CPFAIL>

8.7 Logic Supply Regulator

AMIS-30522 has an on-chip 5V low-drop regulator with external capacitor to supply the digital part of the chip, some low-voltage analog blocks and external circuitry. The voltage is derived from an internal bandgap reference. To calculate the available drive-current for external circuitry, the specified I_{load} should be reduced with the consumption of internal circuitry (unloaded outputs) and the loads connected to logic outputs. See **Error! Reference source not found.**.

8.8 Power-On Reset (POR) Function

The open drain output pin PORB/WD provides an "active low" reset for external purposes. At power-up of AMIS-30522, this pin will be kept low for some time to reset for example an external microcontroller. A small analog filter avoids resetting due to spikes or noise on the VDD supply.

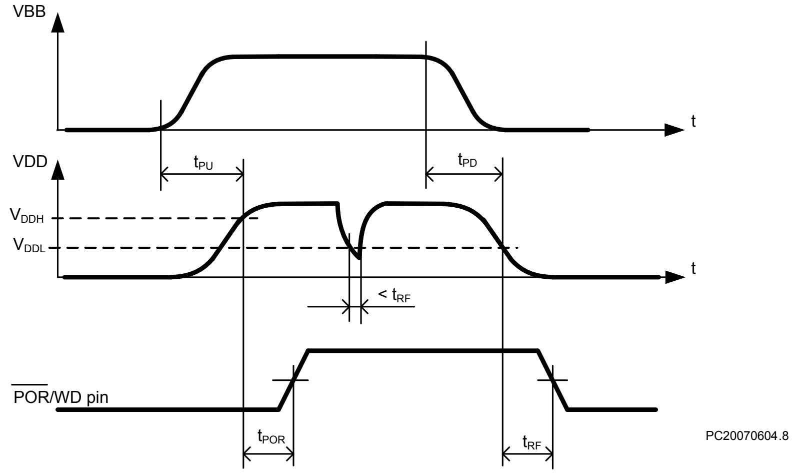


Figure 14: Power-on-Reset Timing Diagram

8.9 Watchdog Function

The watchdog function is enabled/disabled through <WDEN> bit (Table 14). Once this bit has been set to "1" (watchdog enable), the microcontroller needs to re-write this bit to clear an internal timer before the watchdog timeout interval expires. In case the timer is activated and WDEN is acknowledged too early (before t_{WDPR}) or not within the interval (after t_{WDTO}), then a reset of the microcontroller will occur through PORB/WD pin. In addition, a warm/cold boot bit <WD> is available in Table 29 for further processing when the external microcontroller is alive again.

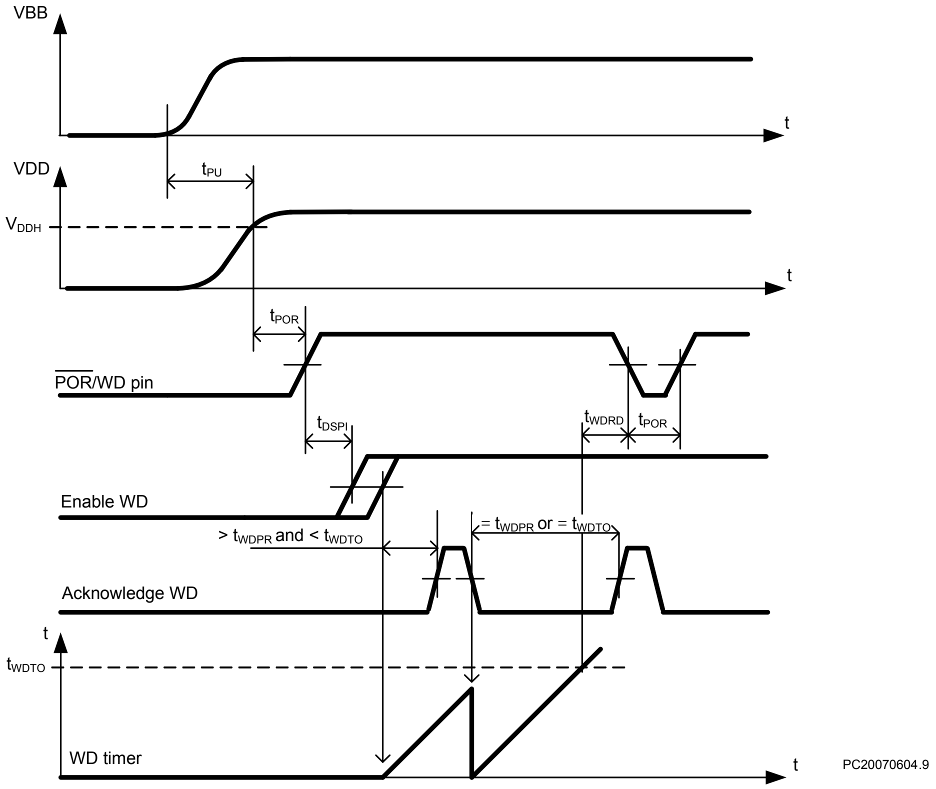


Figure 15: Watchdog Timing Diagram

Note: t_{DSPI} is the time needed by the external microcontroller to shift-in the `<WDEN>` bit after a power-up.

The duration of the watchdog timeout interval is programmable through the `WDT[3:0]` bits (Table 14). The timing is given in Table 13.

Table 13: Watchdog Timeout Interval as Function of WDT[3.0]

Index	WDT[3:0]				t_{WDTO} (ms)
0	0	0	0	0	32
1	0	0	0	1	64
2	0	0	1	0	96
3	0	0	1	1	128
4	0	1	0	0	160
5	0	1	0	1	192
6	0	1	1	0	224
7	0	1	1	1	256
8	1	0	0	0	288
9	1	0	0	1	320
A	1	0	1	0	352
B	1	0	1	1	384
C	1	1	0	0	416
D	1	1	0	1	448
E	1	1	1	0	480
F	1	1	1	1	512

8.10 CLR pin (=Hard Reset)

Logic 0 on CLR pin allows normal operation of the chip. To reset the complete digital inside AMIS-30522, the input CLR needs to be pulled to logic 1 during minimum time given by T_{CLR}. (Table 6). This reset function clears all internal registers without the need of a power-cycle. The operation of all analog circuits is depending on the reset state of the digital, charge pump remains active. Logic 0 on CLR pin resumes normal operation again.

The voltage regulator remains functional during and after the reset and the PORB/WD pin is not activated. Watchdog function is reset completely.

8.11 Sleep Mode

The bit <SLP> in Table 17 is provided to enter a so-called “sleep mode”. This mode allows reduction of current-consumption when the motor is not in operation. The effect of sleep mode is as follows:

- The drivers are put in HiZ
- All analog circuits are disabled and in low-power mode
- All internal registers are maintaining their logic content
- NXT and DIR inputs are forbidden
- SPI communication remains possible (slight current increase during SPI communication)
- Reset of chip is possible through CLR pin
- Oscillator and digital clocks are silent, except during SPI communication

The voltage regulator remains active but with reduced current-output capability ($I_{LOADSLP}$). The watchdog timer stops running and it’s value is kept in the counter. Upon leaving sleep mode, this timer continues from the value it had before entering sleep mode.

Normal operation is resumed after writing logic ‘0’ to bit <SLP>. A start-up time is needed for the charge pump to stabilize. After this time, NXT commands can be issued.

9.0 SPI Interface

The serial peripheral interface (SPI) allows an external microcontroller (Master) to communicate with AMIS-30521. The implemented SPI block is designed to interface directly with numerous micro-controllers from several manufacturers. AMIS-30521 acts always as a Slave and can't initiate any transmission. The operation of the device is configured and controlled by means of SPI registers which are observable for read and/or write from the Master.

9.1 SPI Transfer Format and Pin Signals

During a SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line (CLK) synchronizes shifting and sampling of the information on the two serial data lines (DO and DI). DO signal is the output from the Slave (AMIS-30521), and DI signal is the output from the Master. A chip select line (CSB) allows individual selection of a Slave SPI device in a multiple-slave system. The CSB line is active low. If AMIS-30521 is not selected, DO is pulled up with the external pull up resistor. Since AMIS-30521 operates as a Slave in MODE 0 (CPOL = 0; CPHA = 0) it always clocks data out on the falling edge and samples data in on rising edge of clock. The Master SPI port must be configured in MODE 0 too, to match this operation. The SPI clock idles low between the transferred bytes. The diagram below is both a Master and a Slave timing diagram since CLK, DO and DI pins are directly connected between the Master and the Slave.

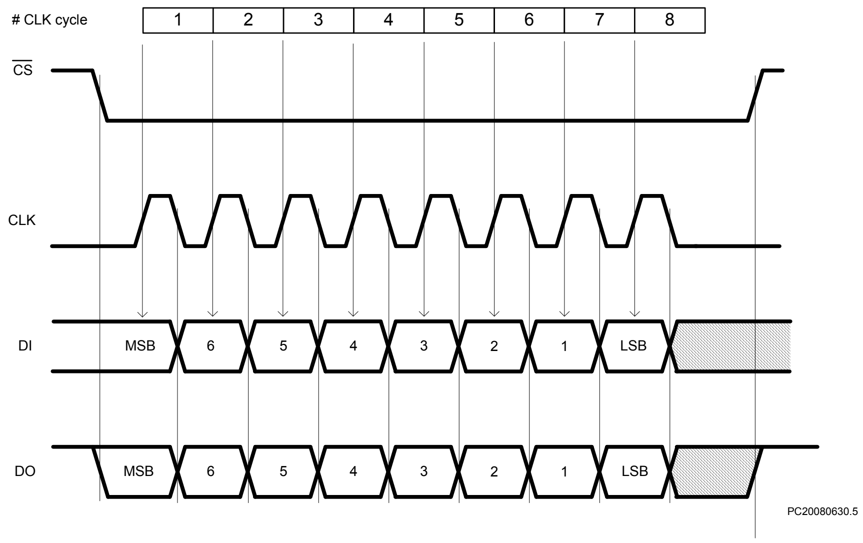


Figure 16: Timing Diagram of a SPI transfer

Note: At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the addressed internal SPI register. The internal SPI registers are updated at the first rising edge of the AMIS-30521 system clock when CSB = High

9.2 Transfer packet:

Serial data transfer is assumed to follow MSB first rule. The transfer packet contains one or more bytes.

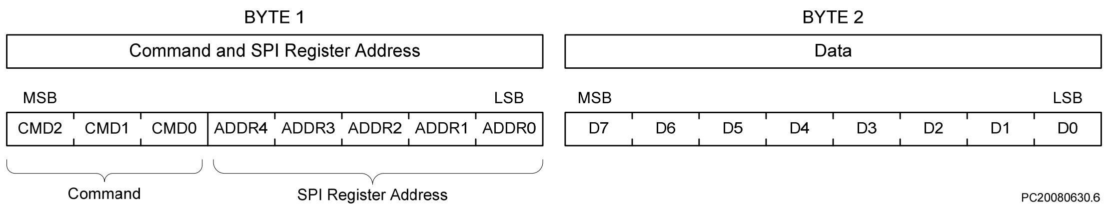


Figure 17: SPI transfer packet

Byte 1 contains the Command and the SPI Register Address and indicates to AMIS-30521 the chosen type of operation and addressed register. Byte 2 contains data, or sent from the Master in a WRITE operation, or received from AMIS-30521 in a READ operation.
2 command types can be distinguished in the communication between master and AMIS-30521:

- READ **from** SPI Register with address ADDR[4:0]: **CMD2** = "0"
- WRITE **to** SPI Register with address ADDR[4:0]: **CMD2** = "1"

9.2.1. READ operation

If the Master wants to read data from Status or Control Registers, it initiates the communication by sending a READ command. This READ command contains the address of the SPI register to be read out. At the falling edge of the eight clock pulse the data-out shift register is updated with the content of the corresponding internal SPI register. In the next 8-bit clock pulse train this data is shifted out via DO pin. At the same time the data shifted in from DI (Master) should be interpreted as the following successive command or is dummy data.

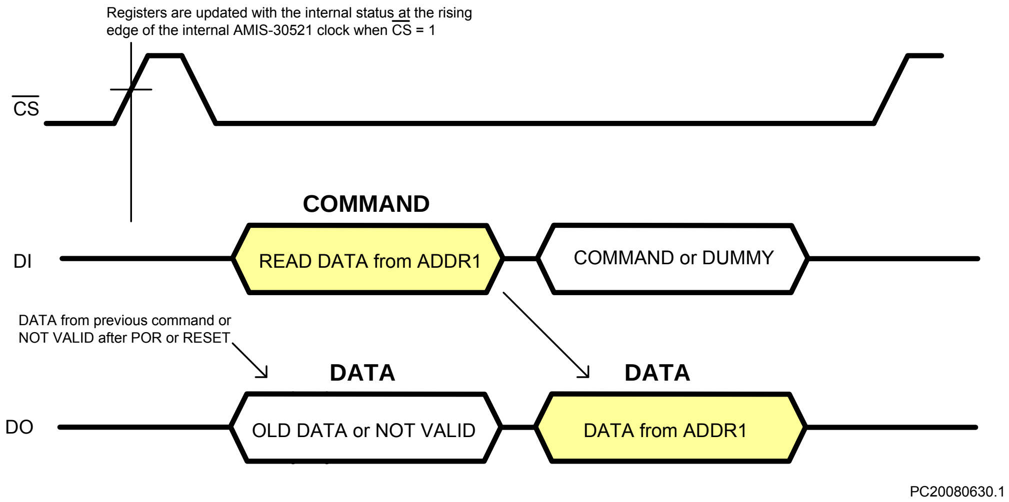


Figure 18: Single READ operation where DATA from SPI register with Address 1 is read by the Master

All 4 Status Registers (see SPI Registers) contain 7 data bits and a parity check bit The most significant bit (D7) represents a parity of D[6:0]. If the number of logical ones in D[6:0] is odd, the parity bit D7 equals "1". If the number of logical ones in D[6:0] is even then the parity bit D7 equals "0". This simple mechanism protects against noise and increases the consistency of the transmitted data. If a parity check error occurs it is recommended to initiate an additional READ command to obtain the status again.

Also the Control Registers can be read out following the same routine. Control Registers don't have a parity check. The CSB line is active low and may remain low between successive READ commands as illustrated in Figure 19. There is however one exception. In case an error condition is latched in one of Status Registers (see SPI Registers) the ERRB pin is activated. (See 8.6.5. Error Output). This signal flags a problem to the external microcontroller. By reading the Status Registers information about the root cause of the problem can be determined. After this READ operation the Status Registers are cleared. Because the Status Registers and ERRB pin (see SPI Registers) are only updated by the internal system clock when the CSB line is high, the Master should force CSB high immediately after the READ operation. For the same reason it is recommended to keep the CSB line high always when the SPI bus is idle

9.2.2. WRITE operation

If the Master wants to write data to a Control Register it initiates the communication by sending a WRITE command. This contains the address of the SPI register to write to. The command is followed with a data byte. This incoming data will be stored in the corresponding Control Register after CSB goes from low to high! AMIS-30521 responds on every incoming byte by shifting out via DO the data stored in the last received address.

It is important that the writing action (command - address and data) to the Control Register is exactly 16 bits long. If more or less bits are transmitted the complete transfer packet is ignored.

A WRITE command executed for a read-only register (e.g. Status Registers) will not affect the addressed register and the device operation.

Because after a power-on-reset the initial address is unknown the data shifted out via DO is not valid.

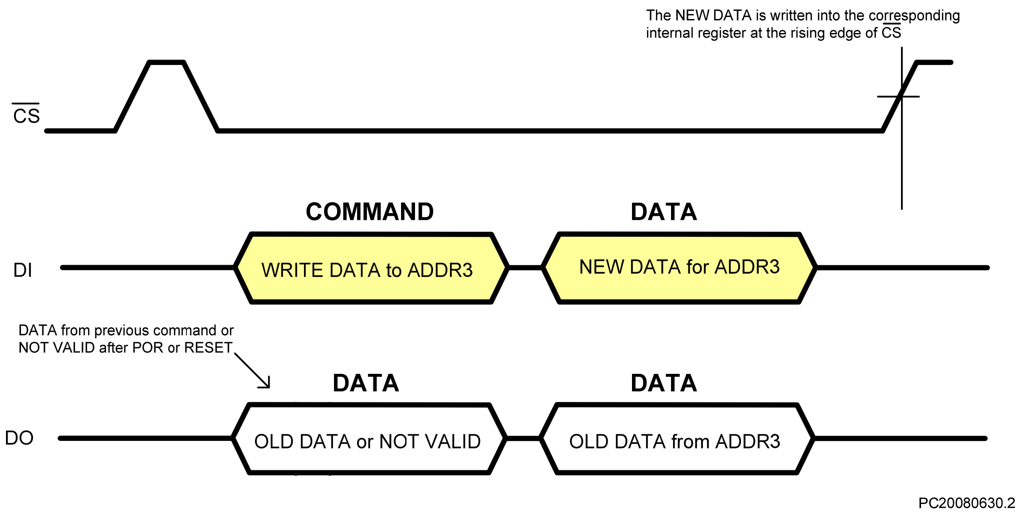


Figure 19: Single WRITE operation where DATA from the Master is written in SPI register with Address 3

9.2.3. Examples of combined READ and WRITE operations

In the following examples successive READ and WRITE operations are combined. In Figure 18 the Master first reads the status from Register at ADDR4 and at ADDR5 followed by writing a control byte in Control Register at ADDR2. Note that during the write command (in Figure 4) the old data of the pointed register is returned at the moment the new data is shifted in

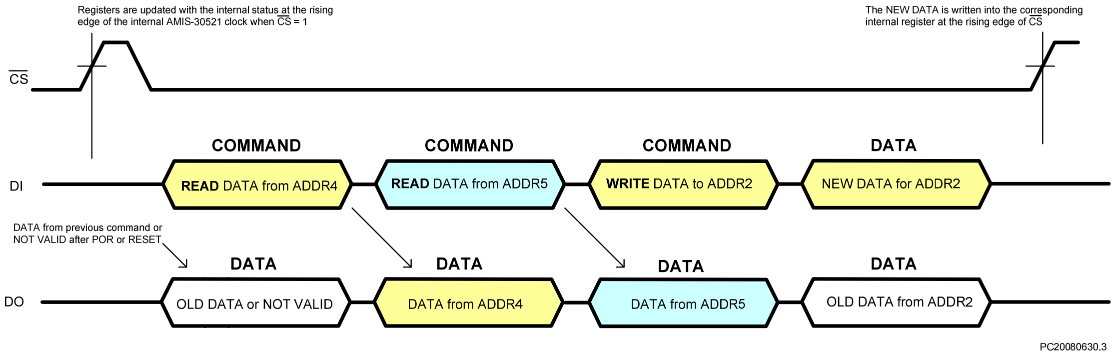


Figure 20: 2 successive READ commands followed by a WRITE command

After the write operation the Master could initiate a read back command in order to verify the data correctly written as illustrated in Figure 19. During reception of the READ command the old data is returned for a second time. Only after receiving the READ command the new data is transmitted. This rule also applies when the master device wants to initiate an SPI transfer to read the Status Registers. Because the internal system clock updates the Status Registers only when CSB line is high, the first read out byte might represent old status information.

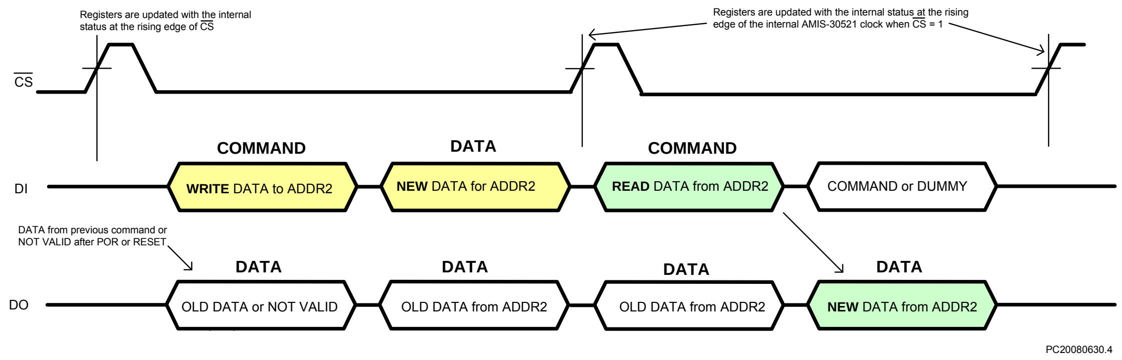


Figure 21: A WRITE operation where DATA from the Master is written in SPI register with Address 2 followed by a READ back operation to confirm a correct WRITE operation

Note: The internal data-out shift buffer of AMIS-30521 is updated with the content of the selected SPI register only at the last (every eight) falling edge of the CLK signal (see SPI Transfer Format and Pin Signals). As a result, new data for transmission cannot be written to the shift buffer at the beginning of the transfer packet and the first byte shifted out might represent old data.

9.3 SPI Control Registers

All SPI control registers have Read/Write Access and default to "0" after power-on or hard reset.

Table 14: SPI Control Register WR

Control Register (WR)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	WDEN	WDT[3:0]				-	-	-

Where:
R/W Read and Write access
Reset: Status after power-On or hard reset
WDEN: Watchdog enable. Writing "1" to this bit will activate the watchdog timer (if not enabled yet) or will clear this timer (if already enabled). Writing "0" to this bit will clear WD bit (Table 29).
WDT[3:0]: Watchdog timeout interval

Table 15: SPI Control Register 0

Control Register 0 (CR0)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	SM[2:0]			CUR[4:0]				

Where:
R/W Read and Write access
Reset: Status after power-On or hard reset
SM[2:0]: Step mode
CUR[4:0]: Current amplitude

Table 16: SPI Control Register 1

Control Register 1 (CR1)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	DIRCTRL	NXTP	-	-	PWMF	PWMJ	EMC[1:0]	

Where:
R/W Read and Write access
Reset:: Status after power-On or hard reset
DIRCTRL Direction control
NXTP NEXT polarity
PWMF PWM frequency
PWMJ PWM jitter
EMC[1:0] EMC slope control

Table 17: SPI Control Register 2

Control Register 2 (CR2)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h	Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Reset	0	0	0	0	0	0	0	0
	Data	MOTEN	SLP	SLAG	SLAT	-	-	-	-

Where:
R/W Read and Write access
Reset: Status after power-On or hard reset
MOTEN Motor enable
SLP Sleep
SLAG Speed load angle gain

SLAT Speed load angle transparency

Table 18: SPI Control Parameter Overview SLAT

Symbol	Description	Status	Behavior
SLAT	Speed load angle transparency bit	<SLAT> = 0	SLA is transparent
		<SLAT> = 1	SLA is NOT transparent

Table 19: SPI Control Parameter Overview SLAG

Symbol	Description	Status	Value
SLAG	Speed load angle gain setting	<SLAG> = 0	Gain = 0.5
		<SLAG> = 1	Gain = 0.25

Table 20: SPI Parameter Overview PWMF

Symbol	Description	Status	Value
PWMF	Enables doubling of the PWM frequency	<PWMF> = 0	f_{PWM} = 22.8kHz
		<PWMF> = 1	f_{PWM} = 45.6kHz

Table 21: SPI Control Parameter Overview PWMJ

Symbol	Description	Status	Behavior
PWMJ	Enables jittery PWM	<PWMJ> = 0	Jitter disabled
		<PWMJ> = 1	Jitter enabled

Table 22: SPI Control Overview SLP

Symbol	Description	Status	Behavior
SLP	Enables sleep mode	<SLP> = 0	Active mode
		<SLP> = 1	Sleep mode

Table 23: SPI Control Parameter Overview MOTEN

Symbol	Description	Status	Value
MOTEN	Activates the motor driver outputs	<MOTEN> = 0	Drivers disabled
		<MOTEN> = 1	Drivers enabled

Table 24: SPI Control Parameter Overview DIRCTRL

Symbol	Description	Status		Value
DIRCTRL	Controls the direction of rotation (in combination with logic level on input DIR)	<DIR> = 0	<DIRCTRL> = 0	CW motion
			<DIRCTRL> = 1	CCW motion
		<DIR> = 1	<DIRCTRL> = 0	CCW motion
			<DIRCTRL> = 1	CW motion

Table 25: SPI Control Parameter Overview NXTP

Symbol	Description	Status	Value
NXTP	Selects if NXT triggers on rising or falling edge	<NXTP> = 0	Trigger on rising edge
		<NXTP> = 1	Trigger on falling edge

CUR[4:0] Selects IMCmax peak. This is the peak or amplitude of the regulated current waveform in the motor coils.

Table 26: SPI Control Parameter Overview CUR[4:0]

Index	CUR[4:0]					Current (mA)	Index	CUR[4:0]					Current (mA)
0	0	0	0	0	0	30	10	1	0	0	0	0	365
1	0	0	0	0	1	60	11	1	0	0	0	1	400
2	0	0	0	1	0	90	12	1	0	0	1	0	440
3	0	0	0	1	1	100	13	1	0	0	1	1	485
4	0	0	1	0	0	110	14	1	0	1	0	0	535
5	0	0	1	0	1	120	15	1	0	1	0	1	595
6	0	0	1	1	0	135	16	1	0	1	1	0	650
7	0	0	1	1	1	150	17	1	0	1	1	1	725
8	0	1	0	0	0	160	18	1	1	0	0	0	800
9	0	1	0	0	1	180	19	1	1	0	0	1	885
A	0	1	0	1	0	200	1A	1	1	0	1	0	970
B	0	1	0	1	1	220	1B	1	1	0	1	1	1070
C	0	1	1	0	0	240	1C	1	1	1	0	0	1190
D	0	1	1	0	1	270	1D	1	1	1	0	1	1300
E	0	1	1	1	0	300	1E	1	1	1	1	0	1450
F	0	1	1	1	1	325	1F	1	1	1	1	1	1600

EMC[1:0] Adjusts the dV/dt of the PWM voltage slopes on the motor pins.

Table 27: SPI Control Parameter Overview EMC[1:0]

Index	EMC[1:0]		Slope (V/µs)	Remark
0	0	0	150	Turn-on and turn-off voltage slope 10% to 90%
1	0	1	100	"
2	1	0	50	"
3	1	1	25	"

`SM[2:0]` Selects the micro-stepping mode.

Table 28: SPI Control Parameter Overview SM[2:0]

Index	SM[2:0]			Step Mode	Remark
0	0	0	0	1/32	Micro-step
1	0	0	1	1/16	Micro-step
2	0	1	0	1/8	Micro-step
3	0	1	1	¼	Micro-step
4	1	0	0	½	Uncompensated half-step
5	1	0	1	½	Compensated half-step
6	1	1	0	Full	Full step
7	1	1	1	N/A	For future use

9.4 SPI Status Register Description

All four SPI status registers have Read Access and are default to "0" after power-on or hard reset.

Table 29: SPI Status Register 0

Status Register 0 (SR0)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	TW	CPfail	WD(1)	OPENX	OPENY	-	-

Where:

R	Read only mode access
Reset	Status after power-on or hard reset
PAR	Parity check
TW	Thermal warning
Cpfail	Charge pump failure
WD	Watchdog event
OPENX	Open Coil X detected
OPENY	Open Coil Y detected

Remark: WD(1) – This bit indicates that the watchdog timer has not been cleared properly. If the master reads that WD is set to "1" after reset, it means that a watchdog reset occurred (warm boot) instead of POR (cold boot). WD bit will be cleared only when the master writes "0" to WDEN bit. (Table 14).

Data is **not** latched

Table 30: SPI Status Register 1

Status Register 1 (SR1)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	OVCXPT	OVCXPB	OVCXNT	OVCXNB	-	-	-

Where:
R Read only mode access
Reset Status after power-on or hard reset
PAR Parity check
OVXPT Over-current detected on X H-bridge: MOTXP terminal, top transistor
OVXPB Over-current detected on X H-bridge: MOTXP terminal, bottom transistor
OVXNT Over-current detected on X H-bridge: MOTXN terminal, top transistor
OVXNB Over-current detected on X H-bridge: MOTXN terminal, bottom transistor

Remark: Data is latched

Table 31: SPI Status Register 2

Status Register 2 (SR2)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	OVCYPT	OVCYPB	OVCYYNT	OVCYNB	TSD	-	-

Where:
R Read only mode access
Reset Status after power-on or hard reset
PAR Parity check
OVCYPT Over-current detected on Y H-bridge: MOTYP terminal, top transistor
OVCYPB Over-current detected on Y H-bridge: MOTYP terminal, bottom transistor
OVCYNT Over-current detected on Y H-bridge: MOTYN terminal, top transistor
OVCYNB Over-current detected on Y H-bridge: MOTYN terminal, bottom transistor
TSD Thermal shutdown

Remark: Data is latched

Table 32: SPI Status Register 3

Status Register 3 (SR3)									
Address	Content	Structure							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h	Access	R	R	R	R	R	R	R	R
	Reset	0	0	0	0	0	0	0	0
	Data	PAR	MSP[6:0]						

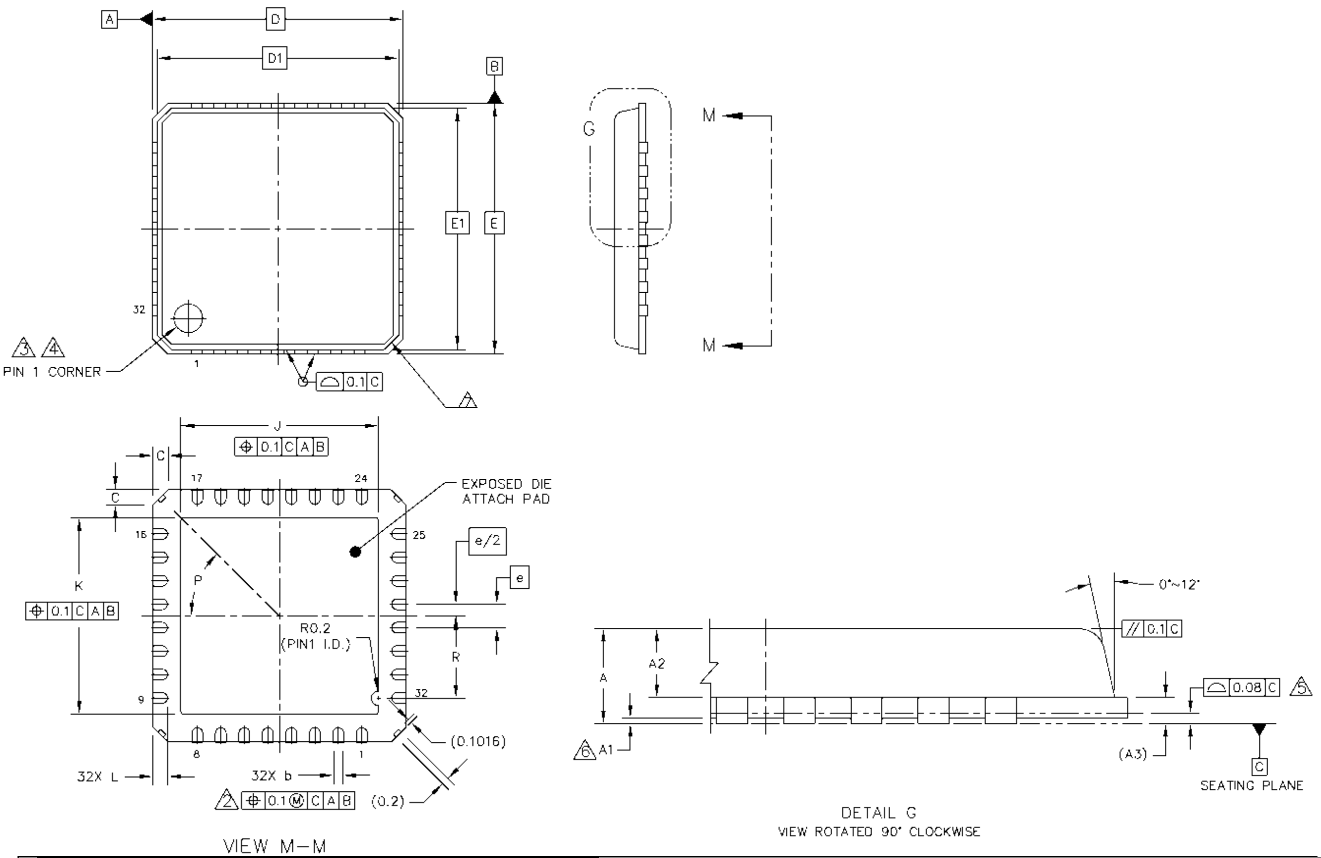
Where:
R Read only mode access
Reset Status after power-on or hard reset
PAR Parity check
MSP[6:0] Translator micro-step position

Remark: Data is **not** latched

Table 33: SPI Status Flags Overview

Flag	Mnemonic	Length (bit)	Related SPI Register	Comment	Reset State
Charge pump failure	CPFail	1	Status Register 0	'0' = no failure '1' = failure: indicates that the charge pump does not reach the required voltage level. Note 1	'0'
Micro-step position	MSP[6:0]	7	Status Register 3	Translator micro step position	'0000000'
OPEN Coil X	OPENX	1	Status Register 0	'1' = Open coil detected	'0'
OPEN Coil Y	OPENY	1	Status Register 0	'1' = Open coil detected	'0'
OVer **C**urrent on X H-bridge; MOT**XN** terminal; **B**ottom tran.	OVCXNB	1	Status Register 1	'0' = no failure '1' = failure: indicates that over current is detected at bottom transistor XN-terminal	'0'
OVer **C**urrent on X H-bridge; MOT**XN** terminal; **T**op transist.	OVCXNT	1	Status Register 1	'0' = no failure '1' = failure: indicates that over current is detected at top transistor XN-terminal	'0'
OVer **C**urrent on X H-bridge; MOT**XP** terminal; **B**ottom tran.	OVCXPB	1	Status Register 1	'0' = no failure '1' = failure: indicates that over current is detected at bottom transistor XP-terminal	'0'
OVer **C**urrent on X H-bridge; MOT**XP** terminal; **T**op transist.	OVCXPT	1	Status Register 1	'0' = no failure '1' = failure: indicates that over current is detected at top transistor XP-terminal	'0'
OVer **C**urrent on Y H-bridge; MOT**YN** terminal; **B**ottom tran.	OVCYNB	1	Status Register 2	'0' = no failure '1' = failure: indicates that over current is detected at bottom transistor YN-terminal	'0'
OVer **C**urrent on Y H-bridge; MOT**YN** terminal; **T**op transist.	OVCYNT	1	Status Register 2	'0' = no failure '1' = failure: indicates that over current is detected at top transistor YN-terminal	'0'
OVer **C**urrent on Y H-bridge; MOT**YP** terminal; **B**ottom tran.	OVCYPB	1	Status Register 2	'0' = no failure '1' = failure: indicates that over current is detected at bottom transistor YP-terminal	'0'
OVer **C**urrent on Y H-bridge; MOT**YP** terminal; **T**op transist.	OVCYPT	1	Status Register 2	'0' = no failure '1' = failure: indicates that over current is detected at top transistor YP-terminal	'0'
Thermal shutdown	TSD	1	Status Register 2		'0'
Thermal warning	TW	1	Status Register 0		'0'
Watchdog event	WD	1	Status Register 0	'1' = watchdog reset after time-out	'0'

10.0 Package Outline



Dimensions:

Dim	Min	Nom	Max	Unit
A	0.8		0.9	mm
A1	0	0.02	0.05	mm
A2	0.576	0.615	0.654	mm
A3		0.203		mm
b	0.25	0.3	0.35	mm
C	0.24	0.42	0.6	mm
D		7		mm
D1		6.75		mm
E		7		mm
E1		6.75		mm
e		0.65		mm
J	5.37	5.47	5.57	mm
K	5.37	5.47	5.57	mm
L	0.35	0.4	0.45	mm
P		45		Degree
R	2.185		2.385	mm

Notes :

△2 Dimensions apply to plated terminal and are measured between 0.2 and 0.25 mm from terminal tip.

△3 The pin #1 indication must be placed on the top surface of the package by using indentation mark or other feature of package body.

△4 Exact shape and size of this feature is optional

△5 Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.

△6 Applied only to terminals

△7 Exact shape of each corner is optional

7x7 NQFP

Figure 22: NQFP-32: No Lead Quad Flat Pack; 32 Pins; Body Size 7x7mm (AMIS Reference: NQFP-32)

11.0 Soldering

11.1 Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in the AMIS "Data Handbook IC26; Integrated Circuit Packages" (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards (PCB) with high population densities. In these situations re-flow soldering is often used.

11.2 Re-flow Soldering

Re-flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the PCB by screen printing, stencilling or pressure-syringe dispensing before package placement. Several methods exist for re-flowing; for example, infrared/convection heating in a conveyor type oven.

Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on the heating method. Typical re-flow peak temperatures range from 215 to 260°C. The top-surface temperature of the packages should preferably be kept below 230°C.

11.3 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or PCBs with a high component density, as solder bridging and non-wetting can present major problems. To overcome these problems, the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the PCB;
  - Smaller than 1.27mm, the footprint longitudinal axis must be parallel to the transport direction of the PCB. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45º angle to the transport direction of the PCB. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

11.4 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270 and 320°C.

Table 34: Soldering Process

Package	Soldering Method	
	Wave	Re-flow (1)
BGA, SQFP	Not suitable	Suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	Not suitable (2)	Suitable
PLCC (3) , SO, SOJ	Suitable	Suitable
LQFP, QFP, TQFP	Not recommended (3) (4)	Suitable
SSOP, TSSOP, VSO	Not recommended (5)	Suitable

Notes:

(1) All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the drypack information in the "Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods."

(2) These packages are not suitable for wave soldering as a solder joint between the PCB and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).

(3) If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

(4) Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65mm.

(5) Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5mm.

12.0 Document History

Table 35: Revision History

Revision	Date	Modification
0.1	18-Jan-06	Initial draft
0.2	24-Jan-06	Draft: changed PWM description, added SLA pin description, changed POR and WD paragraphs.
0.3	9-Feb-06	CEN->CENB, NXT pin timing, SPI I/F, 30522 section 8.5, 8.6,8.7, 30522 section 8.4,8.5
0.4	9-Mar-06	Updated pin-out & added drawing, CENB->CLR, ERR->ERRB, removed SWP bits, updated SPI bits, added package details
0.5	22-Mar-06	Renamed CS -> CSB, Swapped pins CLR and CSB
0.6	24-May-06	Updated pins, AC&DC tables, SLA specs, SM[2:0] decoding
1.0	6-June-07	Final version derived from common 30521/30522 datasheet
2.0	3-July-08	Move content into ON Semiconductor template; update OPN table, AC&DC tables, Application Schematic, SPI interface, SPI registers, Timing NXT

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